

**Department of Electrical and Computer Engineering**

**Second semester 2020/2021**

**Digital lab ENCS2110**

**Experiment No. 5 - Sequential Logic Circuits**

Abstract :

The aim of the experiment is to distinguish between combinational circuits and sequential circuits , also to build different circuits such as latches, flip flops, registers and counters using Proteus.

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# Theory :

### Sequential

circuits are used for circuits where the output in the previous combinational

circuit is wanted in the next operation, so it contains memory and combination circuits,

to save and process the elements needed.

### B. Latches :

Latches work as a storage, it stores binary data (0,1), and it has types such as :

a. RS Latch :

i. It contains two NOR gates to achieve an active high circuit or by using

two NAND gates to achieve an active low circuit and the input of each

gate depends on the output of the previous operation , it can be improved

using control input.

b. D Latch :

i. It contains an RS latch and an inverter to prevent critical race and make it

easier to use.

### C. Flip Flops:

\*) Flip flops also store data in binary, and it consists of latches.

\*) There is many types of Flip flops and some of these types are :

a. D Flip Flop

b. JK Flip Flop

c. T Flip Flop

### D. Registers :

Registers are digital systems that are a collection of flip flops ; N-bit registers

consist of N-flip flops and it is used to store bits of information. (N is determined on how

many bits is the input).

### E. Counters :

Counters are sequential circuits that are used for counting purposes , they can

count specific event happening in the circuit , the counters are considered to be the widest

application of flip flops , also it is claimed that counters are a special type of registers,

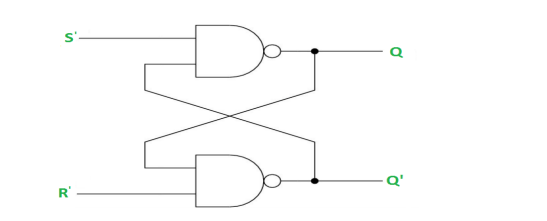
counters have two types (Asynchronous counters (ripple) and Synchronous counters)

# Procedure :

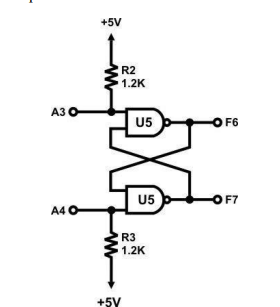
Latches :

### RS Latch :

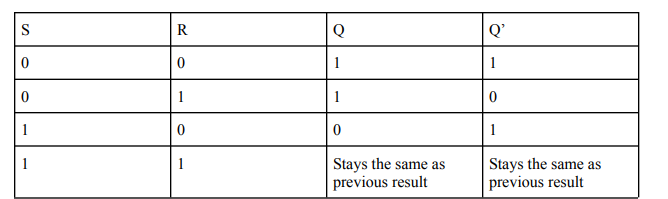
\*) Note : RS latch in the following figure is on low active due to using of nand gates.



### fig(1) : RS Latch



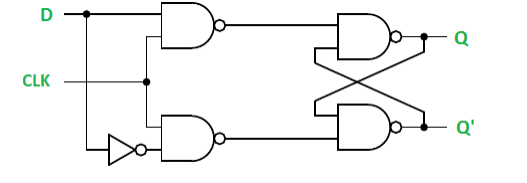
### fig(2) : RS Latch using Proteus



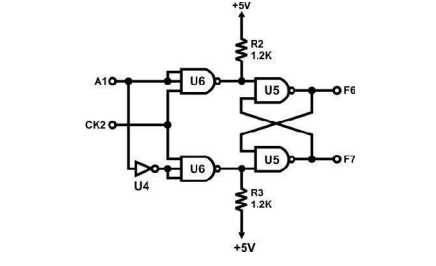
### Truth table (1) : RS latch Active low

## D Latch :

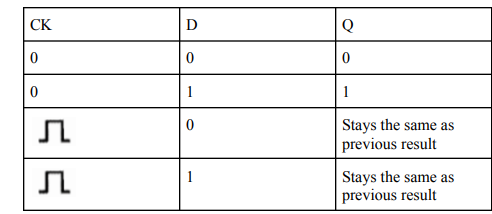
Note: d latch as mentioned in theory before consists of an rs latch and an inverter, also its in low active mode.



#### fig(3) : D Latch

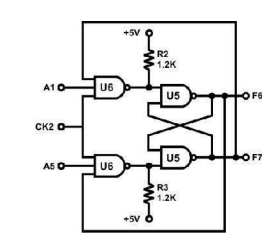


### fig(4) : D Latch using proteus.

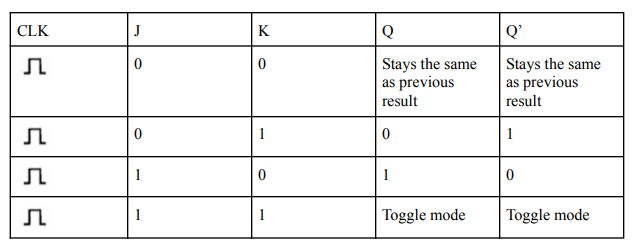


### Truth table (2) : D Latch Active low

## JK Latch :



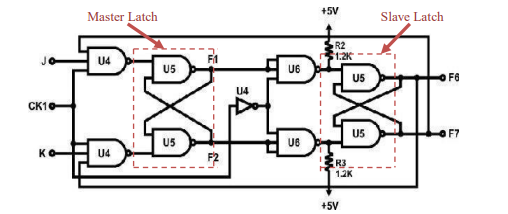
### Figure 5.13: JK Latch



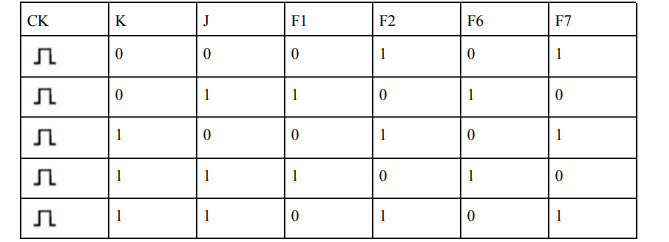
### Truth table (3) : JK latch

## Flip Flops :

### JK Flip flop :



### Fig (6) : Master-Slave JK flip flop



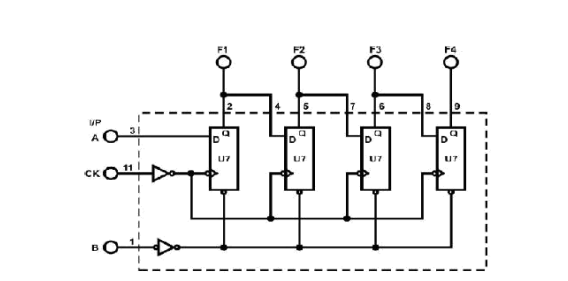
### Truth table (4) : Master-Slave JK flip flop (different cases)

The master-slave circuit mainly consisted of two JK latches and a clock , the slave JK latch(the second one) depends on the output of the master JK latch (the first one) and it is isolated when the clock value is ‘1’.

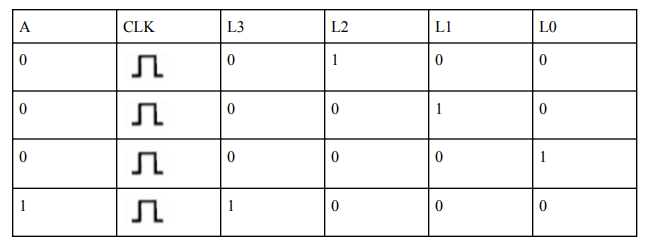
## Registers :

### Shift register :

As recommended this register shifts the value of ‘1’ to the right. Also it is constructed using DTFF.

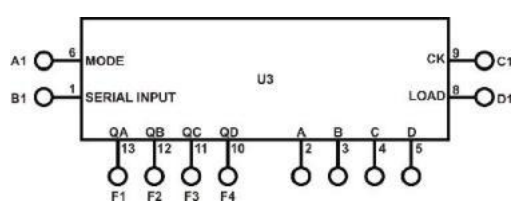


### fig(7) : Shift register

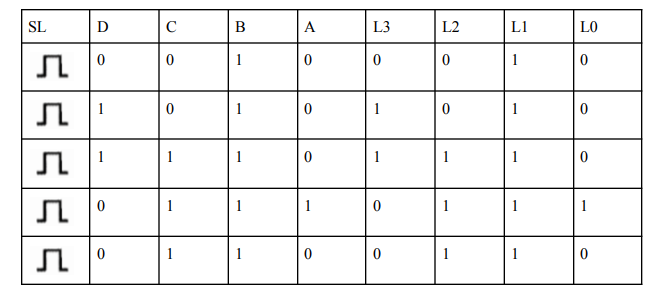


### Truth Table (5) : Shift register

### 4-bit shift register with serial and parallel load :



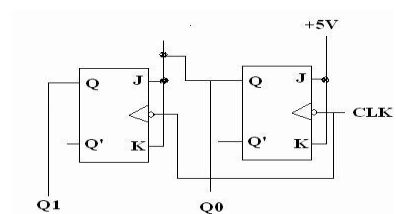
### Figure 5.16: shift register with serial and parallel load



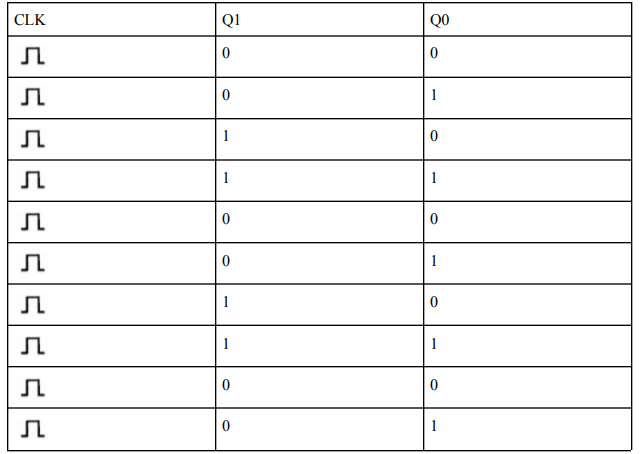
### Truth table (6): shift register with serial and parallel load

## Counters :

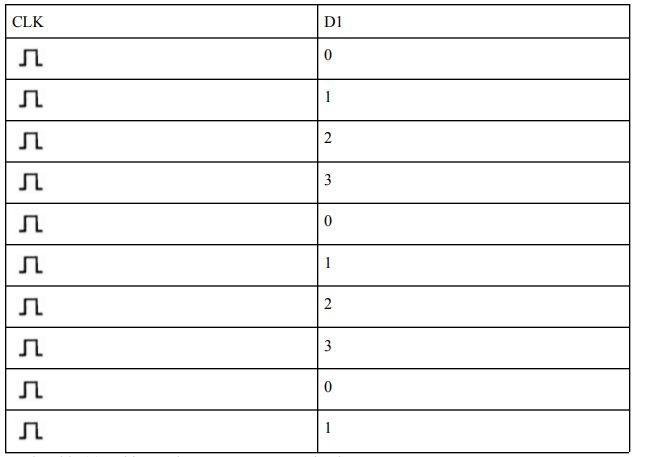
### 2-bit Synchronous Counter :



### Fig (10) : 2-bit Synchronous Counter



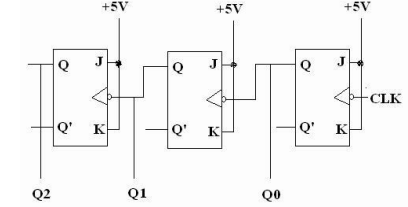
### Truth Table (7) : 2-bit Synchronous Counter Binary



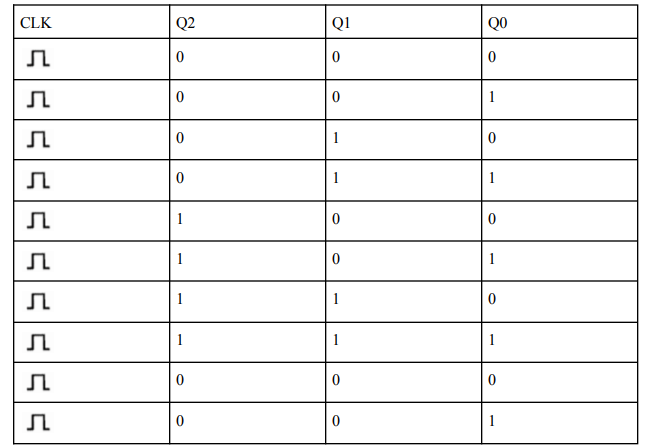
### Truth Table (8): 2-bit Synchronous Counter Decimal

### \*) this counter counts to 3 then reset (maximum value of it is 3).

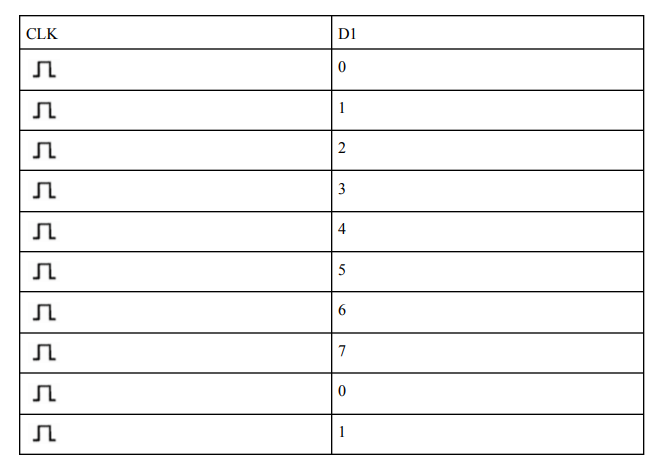
### 3-bit (divide-by-eight) Ripple Counter :



### Fig(11) : 3-bit Ripple Counter



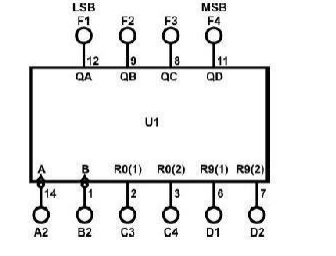
### Truth Table (9) : 3-bit Ripple Counter in Binary



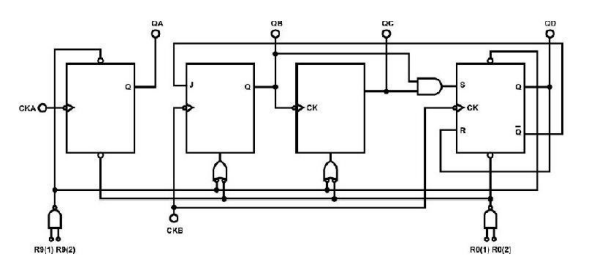
### Truth Table (10) : 3-bit Ripple Counter in Decimal

\*) Reaches 7 then restart from 0 (7 maximum value)

## BCD Counter :



### Fig (12) : BCD Counter

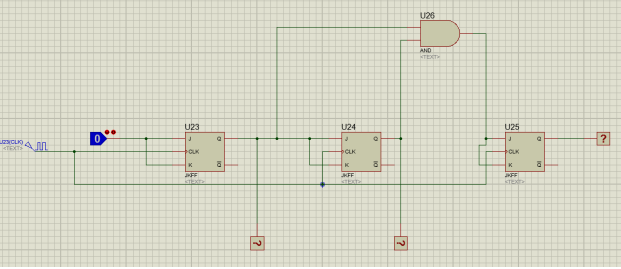


### IC 7490 BCD Counter

\*) this counter counts to 9 then reset to 0 infinitely.

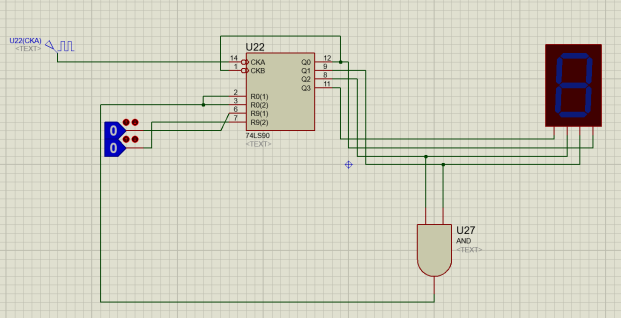
# Tasks :

## Task 2 :

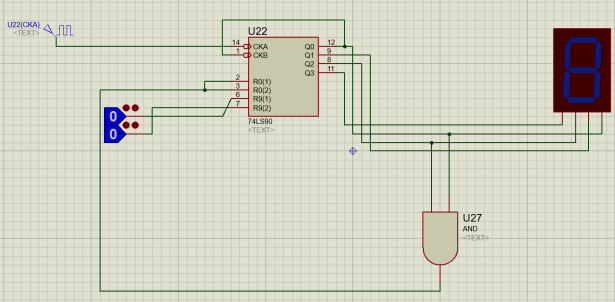


### Fig (13) : Figure 18 : 3-bit Synchronous counter

### Task 3 :

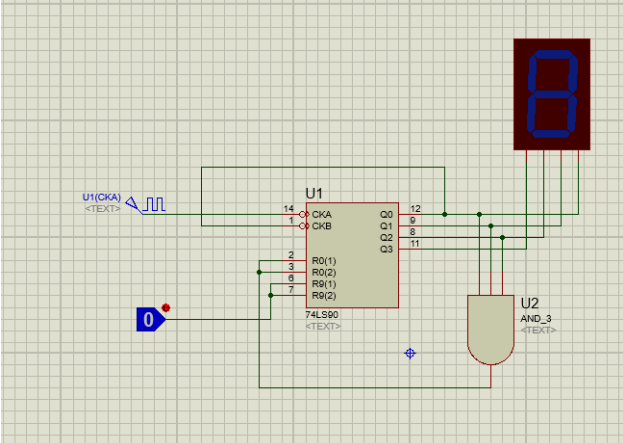


### Fig (14) : 0 to 5 counter



### Fig (15) : 0 to 4 counter

## To-Do :



### Fig (16) : 0 to 6 counter

\*) The main idea that in any counter we need to construct using (7490) we need to know the maximum value like 6 in this to-do, then we should connect the next value of maximum (7) to the reset 0 nodes, so it keeps counting to 6 and when it reaches 7 or 0111 (in Binary) the reset will start again from 0.

# Discussion :

● Latches are level sensitive so its output might be not accurate because of the change of the output in every pulse of the clock making reading from latches difficult, so they are rarely used.

● It has an invalid case when both inputs equals one that leads to producing an output for Q to 1 and Q` to 1 as well.

● The main difference between ripple and synchronous is that in a ripple counter every flip flop in the counter is affected by different clocks and each sequential element is triggered differently , however in synchronous counters flip flops share the same clock, so that makes synchronous counters faster than ripple counters.

# Conclusion :

In conclusion, this experiment defined differences between combinational and sequential circuits, and constructing elements such as latches , flip flops, registers and counters to use them to build more complex sequential circuits, also the experiment gave a differentiation between synchronous and asynchronous (ripple) counters.

# References :

● <https://www.geeksforgeeks.org/latches-in-digital-logic/> (22/3/2021 6:32PM)

● <https://en.wikipedia.org/wiki/Flip-flop_(electronics)> (22/3/2021 8:14PM).

● <https://www.javatpoint.com/registers-in-digital> electronics#:~:text=A%20Register%20is%20a%20collection,

n%20number%20of%20flip%20flops. (23/3/2021 5:48PM).

● <https://en.wikipedia.org/wiki/Shift_register> (23/3/2021 6:19PM).

● <https://www.geeksforgeeks.org/counters-in-digital-logic/> (23/3/2021 10:53PM).

● <https://www.geeksforgeeks.org/differences-between-synchronous-and-asynchronous-counter/#:~:text=In%20>

Asynchronous%20Counter%20is%20also,than%20asynchronous%20counter%20in%20operation. (24/3/2021 7:08PM).

● Digital Electronics and Computer Organization Lab textbook.